**I2S\_out.v Document – Zachary Nelson**

**Interfaces:**

|  |  |  |  |
| --- | --- | --- | --- |
| Signal Name | Direction | Bits | Comment |
| clk | in | 1 | Clock |
| rst | in | 1 | Reset |
| dout\_lft | in | 16 | Left Parallel Digital Audio |
| dout\_rgt | in | 16 | Right Parallel Digital Audio |
| dout\_rts | in | 1 | Ready to Send |
| sck | out | 1 | Digital Audio Bit Clock (max of 48kHz) |
| ws | out | 1 | Word Select (Left/Right Audio Channel) |
| sd | out | 1 | Digital Audio Serial Data |
| dout\_rtr | out | 1 | Ready to Receive |
| fifo\_underrun | out | 1 | Output Audio FIFO Underrun |

**Functional Requirements:**

* Data Plane Requirements:
* Control Plane Requirements:
  + Serial data is transmitted in two’s complement with the Most Significant Bit (MSB) first. Serial data must be latched into the receiver on the leading edge of the serial clock signal. See Section 3.1 of I2S Specification Sheet for more details.
  + The buffer sizing will have 16 storage elements which means we need a pointer that is 4 bits.
  + Overflow/Underflow is a possibility because of the FIFO buffer. In either case, the input or output will be ignored and the buffer will not change.
* Control and Status Interface Bit Descriptions:
  + Control Bits
    - ws:
  + Status Bits
    - fifo\_overrun: The FIFO buffer is full and no more audio can be added
    - fifo\_underrun: The FIFO buffer is empty so there is no audio to output
    - din\_rtr: Read client asserts ready to receive
    - din\_rts:
    - dout\_rtr:
    - dout\_rts:

**Micro-Architecture:**

* Sub-blocks
  + fifo.v
* Block Diagram

**Design:**

**Verification:**

Testbench:

Test Plan: